Customer No.: 31561
Application No.: 10/709,849
Docket NO.: 12920-US-PA

AMENDMENTS

In the Claims:

1. (currently amended) A driving circuit of a liquid crystal display, comprising:

a plurality of gate drivers, for selectively driving a plurality of thin film transistors of the liquid crystal display;

a plurality of source drivers, for receiving an image signal, the plurality of source drivers cooperating with the plurality of gate drivers to display an image on the liquid crystal display, each of the ~~plurality of~~ source drivers further comprising an adjustable common voltage generating circuit, each [[the]] adjustable common voltage generating circuit compensating[[,]] a common voltage output from each [[the]] adjustable common voltage generating circuit to make each [[the]] common voltage output from each [[the]] adjustable common voltage generating circuit the same or to make each [[the]] common voltage output to an ITO layer of a panel of the liquid crystal display the same[[,]] based on a common voltage adjustable data and a clock signal; and

a timing sequence controller, for providing a control signal and a data flow to the ~~plurality of~~ gate drivers and the ~~plurality of~~ source drivers and providing the common voltage adjustable data to each [[the]] adjustable common voltage generating circuit.

2. (original) The driving circuit of claim 1, wherein the adjustable common voltage generating circuit comprises:

a digital interface, for receiving the common voltage adjustable data and the clock signal;

a digital to analog converter, coupled to the digital interface, for generating an analog signal based on the common voltage adjustable data; and

an output buffer, coupled to the digital to analog converter, for generating the common voltage based on the analog signal to drive a load of the common voltage.

3. (original) The driving circuit of claim 2, wherein the digital interface comprises at least one of a serial digital interface, a parallel digital interface, a single-ended digital interface and a differential digital interface.

4. (original) The driving circuit of claim 2, wherein the digital interface comprises a shift register.

5. (original) The driving circuit of claim 2, wherein the digital interface comprises a latch.

6. (original) The driving circuit of claim 2, wherein the output buffer comprises an operational amplifier.

7. (original) The driving circuit of claim 2, wherein the timing sequence

controller comprises:

a timing sequence control unit, for providing the control signal and the data flow; and

a common voltage adjustable data generating unit, coupled to the timing sequence control unit, for generating the common voltage adjustable data.

8. (original) The driving circuit of claim 7, wherein an operational timing sequence for the common voltage adjustable data generating unit is controlled by the timing sequence control unit.

9. (original) The driving circuit of claim 7, wherein the common voltage adjustable data generating unit comprises:

a processing unit, for obtaining an optimum common voltage data based on an input data to generate the common voltage adjustable data;

a storage unit, coupled to the processing unit, for storing the optimum common voltage data; and

an interface unit, coupled to the processing unit, for outputting the common voltage adjustable data to the adjustable common voltage generating circuit.

10. (currently amended) A driving circuit of a liquid crystal display, comprising:

a plurality of gate drivers, for selectively driving a plurality of thin film transistors of the liquid crystal display, each of the ~~plurality of~~ gate drivers comprising a first adjustable common voltage generating circuit, each [[the]] first adjustable common voltage generating circuit compensating[[,]] a common voltage output from each [[the]] first adjustable common voltage generating circuit to make each [[the]] common voltage output from each [[the]] first adjustable common voltage generating circuit the same or to make each [[the]] common voltage output to an ITO layer of a panel of the liquid crystal display the same[[,]] based on a common voltage adjustable data and a clock signal;

a plurality of source drivers for receiving an image signal, the ~~plurality of~~ source drivers cooperating with the ~~plurality of~~ gate drivers to display an image on the liquid crystal display, each of the ~~plurality of~~ source drivers further comprising a second adjustable common voltage generating circuit, each [[the]] second adjustable common voltage generating circuit compensating[[,]] a common voltage output from each [[the]] second adjustable common voltage generating circuit to make each [[the]] common voltage output from each [[the]] second adjustable common voltage generating circuit the same or to make each [[the]] common voltage output to an ITO layer of a panel of the liquid crystal display the same[[,]] based on [[a]] <u>the</u> common voltage adjustable data and [[a]] <u>the</u> clock signal; and

a timing sequence controller for providing a control signal and a data flow to the ~~plurality of~~ gate drivers and the ~~plurality of~~ source drivers and providing the common voltage adjustable data to each [[the]] first and second adjustable common voltage generating circuits.

11. (original) The driving circuit of claim 10, wherein each of the first and second adjustable common voltage generating circuits comprises:

a digital interface, for receiving the common voltage adjustable data and the clock signal;

a digital to analog converter, coupled to the digital interface, for generating an analog signal based on the common voltage adjustable data; and

an output buffer, coupled to the digital to analog converter, for generating the common voltage based on the analog signal to drive a load of the common voltage.

12. (original) The driving circuit of claim 11, wherein the digital interface comprises at least one of a serial digital interface, a parallel digital interface, a single-ended digital interface and a differential digital interface.

13. (original) The driving circuit of claim 11, wherein the digital interface comprises a shift register.

14. (original) The driving circuit of claim 11, wherein the digital interface

comprises a latch.

15. (original) The driving circuit of claim 11, wherein the output buffer comprises an operational amplifier.

16. (original) The driving circuit of claim 11, wherein the timing sequence controller comprises:

a timing sequence control unit, for providing the control signal and the data flow; and

a common voltage adjustable data generating unit, coupled to the timing sequence control unit, for generating the common voltage adjustable data.

17. (original) The driving circuit of claim 16, wherein an operational timing sequence for the common voltage adjustable data generating unit is controlled by the timing sequence control unit.

18. (original) The driving circuit of claim 16, wherein the common voltage adjustable data generating unit comprises:

a processing unit, for obtaining an optimum common voltage data based on an input data to generate the common voltage adjustable data;

a storage unit, coupled to the processing unit, for storing the optimum common voltage data; and

an interface unit, coupled to the processing unit, for outputting the common

voltage adjustable data to the first and second adjustable common voltage generating circuits.